



Title of Change:	Datasheet change
Effective date:	16 Nov 2019
Contact information:	Contact your local ON Semiconductor Sales Office or Ondrej.Kupcik@onsemi.com
Type of notification:	This Product Bulletin is for notification purposes only. ON Semiconductor will proceed with implementation of this change upon publication of this Product Bulletin.
Change Category:	Datasheet change
Change Sub-Category(s):	Datasheet/Product Doc change

Sites Affected:

ON Semiconductor Sites	External Foundry/Subcon Sites
None	None

Description and Purpose:

- Device description updated
- Feature list updated

rev.0:

rev.1:

NCV7450

CAN + LDO + HS Driver System Basis Chip

The system basis chip (SBC) NCV7450 integrates +5 V / 250 mA LDO with a high-speed CAN transceiver and one high-side driver with diagnostics, directly controlled by dedicated pins.

Features

- 5 V \pm 2% / 250 mA LDO
 - ◆ Current Limitation
 - ◆ Output Voltage Monitoring
- One High-Speed CAN Transceiver
 - ◆ Current Limitation, Reverse Current Protected
 - ◆ Compliant to ISO11898-2:2016
 - ◆ TxDC Time-out
- One High-Side Driver
 - ◆ R_{dson} = 300 m Ω @ 25°C
 - ◆ Current Limitation
 - ◆ Diagnostic Output
 - ◆ Over-Current Protection
 - ◆ Under-Load Detection

System Basis Chip with CAN FD, LDO Regulator and HS Driver

NCV7450

The system basis chip (SBC) NCV7450 integrates +5 V / 250 mA LDO regulator with a high-speed CAN FD transceiver and one high-side driver with diagnostics, directly controlled by dedicated pins.

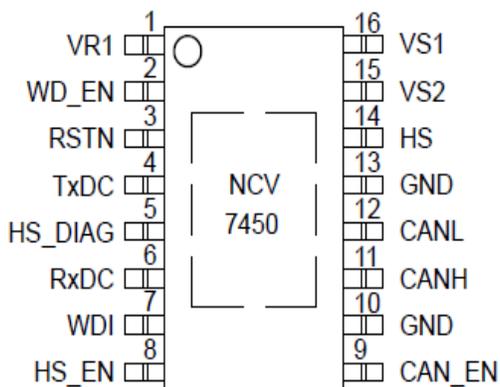
Features

- 5 V \pm 2% / 250 mA LDO
 - ◆ Current Limitation with Fold-back
 - ◆ Output Voltage Monitoring
- One High-Speed CAN FD Transceiver
 - ◆ Current Limitation, Reverse Current Protected
 - ◆ Compliant to ISO11898-2:2016
 - ◆ CAN FD Timing Specified up to 5 Mbit/s
 - ◆ TxDC Timeout
- One High-Side Driver
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 - ◆ Overcurrent Protection
 - ◆ Underload Detection



- Pin connection drawing added

PIN CONNECTIONS



- Application diagram updated

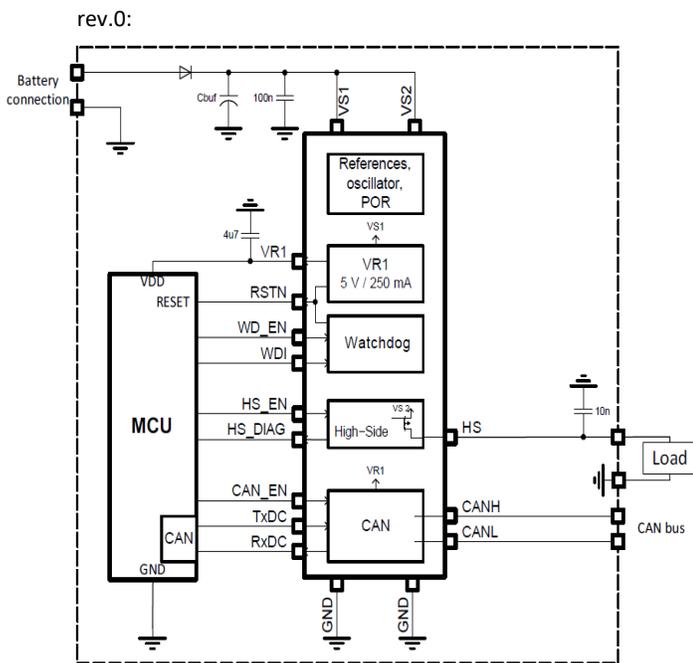


Figure 1. Simplified Application Diagram

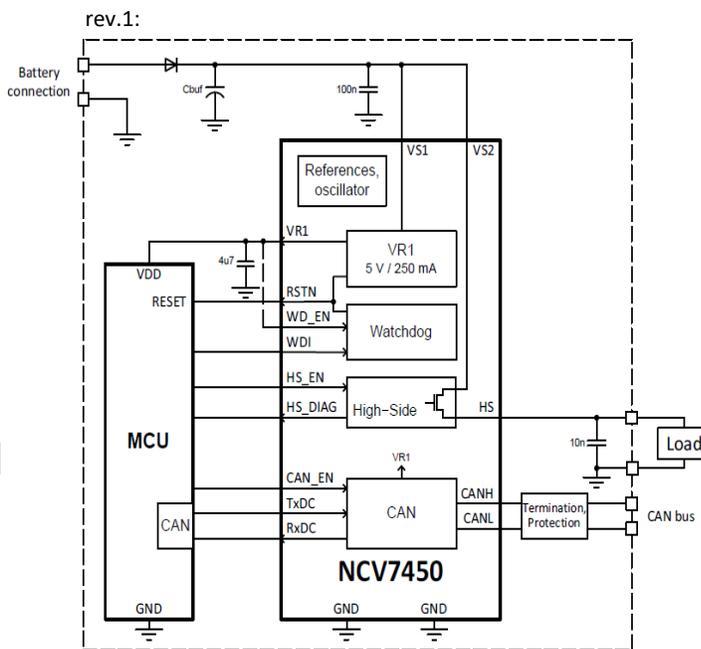
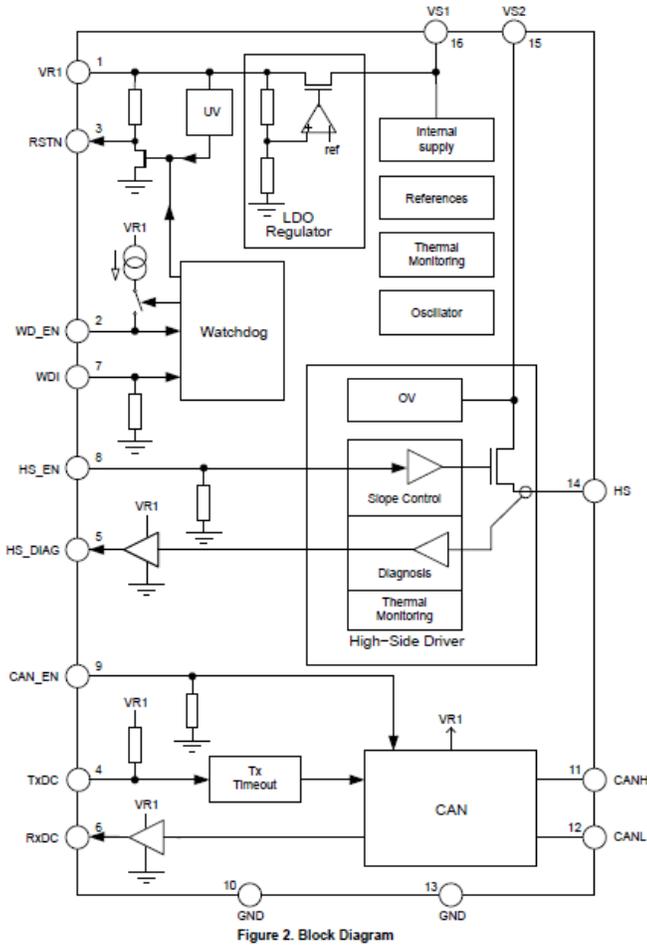


Figure 1. Simplified Application Diagram



- Internal block diagram drawing added



- Peak soldering temperature added

Tsld	Peak Soldering Temperature (Note 3)	260	°C
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- CANH/CANL pins recommended operating range extended

rev.0:

CANH, CANL	CAN bus pins voltage	0	VR1	V
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rev.1:

CANH, CANL	CAN bus pins voltage	-40	40	V
------------	----------------------	-----	----	---

- Ron_HS test condition modified

rev.0:

Ron_HS	On-resistance	Tj = 25°C (Note 6)	0.3	Ω
		Tj = 125°C (Note 6)	0.6	
		Tj = 125°C, Vs2 = 4.3 V (Note 6)	0.8	
		Tj = 150°C	0.7	



rev.1:

Ron_HS	On-resistance	T _J = 25°C (Note 6)	-	0.3	-	Ω
		T _J = 125°C	-	-	0.6	
		T _J = 125°C, Vs2 = 4.3 V (Note 6)	-	-	0.8	
		T _J = 150°C	-	-	0.7	

- twake_filt test condition added

rev.0:

t _{wake_filt}	Dominant time for wake-up via bus		0.15	-	1.8	μs
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rev.1:

t _{wake_filt}	Dominant time for wake-up via bus	CAN_EN = low	0.15	-	1.8	μs
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- Editorial changes

The change will not impact form, fit, or function of product.

List of Affected Standard Parts:

Note: Only the standard (off the shelf) part numbers are listed in the parts list. Any custom parts affected by this PCN are shown in the customer specific PCN addendum in the PCN email notification, or on the [PCN Customized Portal](#).

NCV7450DB0R2G		
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Japanese translation of the notification starts here.
通知の日本語訳はここから始まります。

Note: The Japanese version is for reference only. In case of any differences between the English and Japanese version, the English version shall control.

注：日本語版は参照用です。英語版と日本語版の違いがある場合は、英語版が優先されます。



変更件名:	データシートの変更
発効日:	16 Nov 2019
連絡先情報:	現地のオン・セミコンダクター営業所または <Ondrej.Kupcik@onsemi.com> にお問い合わせください。
通知種別:	本製品速報は通知目的のもののみです。オン・セミコンダクターは本製品速報の発行により本変更を実行します。
変更カテゴリ:	データシートの変更
変更サブカテゴリ:	データシート/製品ドキュメントの変更

影響を受ける拠点:

オン・セミコンダクター拠点:

なし

外部製造工場 / 下請業者拠点:

なし

説明および目的

- 製品の説明が更新されました
- 更新された機能リスト

rev.0:

rev.1:

NCV7450

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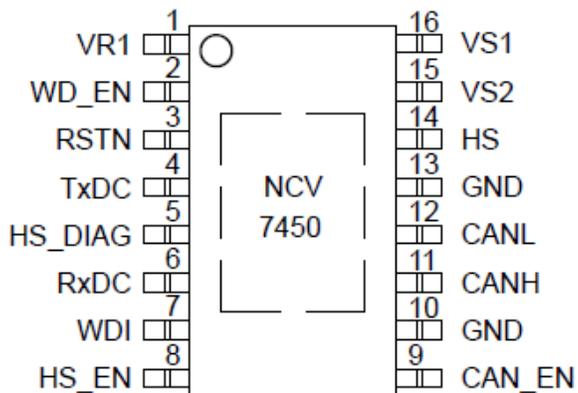
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 - ◆ Current Limitation with Fold-back
 - ◆ Output Voltage Monitoring
- One High-Speed CAN FD Transceiver
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 - ◆ Current Limitation
 - ◆ Diagnostic Output
 - ◆ Overcurrent Protection
 - ◆ Underload Detection



- 追加されたピン接続図

PIN CONNECTIONS



- アプリケーション図が更新されました

rev.0:

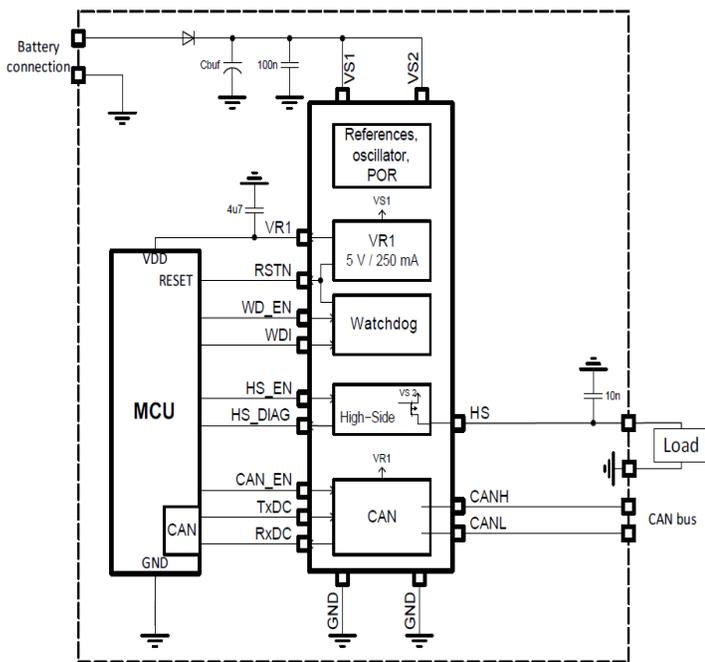


Figure 1. Simplified Application Diagram

rev.1:

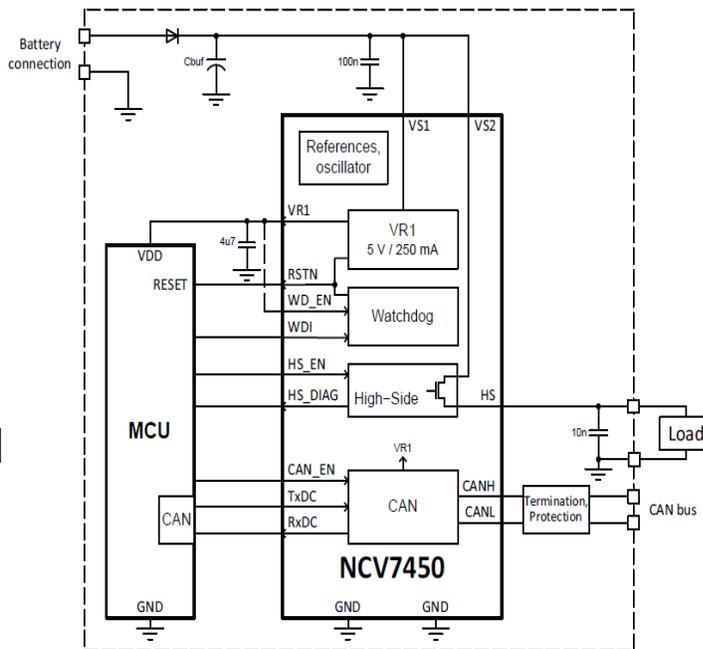


Figure 1. Simplified Application Diagram



● 内部ブロック図の追加

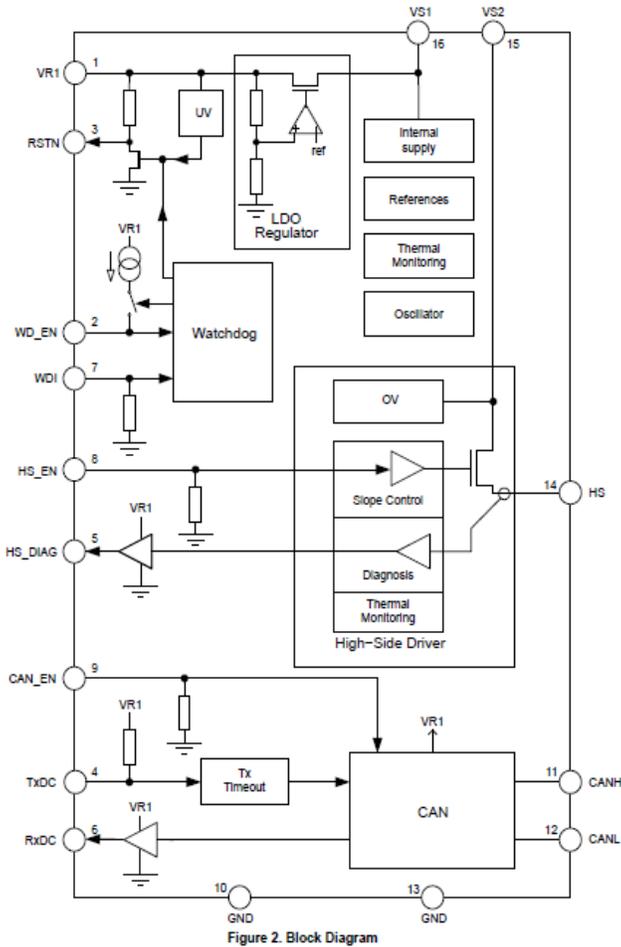


Figure 2. Block Diagram

● はんだ付けピーク温度が追加されました

Tsld	Peak Soldering Temperature (Note 3)	260	°C
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● CANH/CANL ピン推奨動作範囲の拡張

rev.0:

CANH, CANL	CAN bus pins voltage	0	VR1	V
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rev.1:

CANH, CANL	CAN bus pins voltage	-40	40	V
------------	----------------------	-----	----	---

● 変更された Ron_HS テスト条件



rev.0:

Ron_HS	On-resistance	T _j = 25°C (Note 6)		0.3		Ω
		T _j = 125°C (Note 6)			0.6	
		T _j = 125°C, Vs2 = 4.3 V (Note 6)			0.8	
		T _j = 150°C			0.7	

rev.1:

Ron_HS	On-resistance	T _j = 25°C (Note 6)	-	0.3	-	Ω
		T _j = 125°C	-	-	0.6	
		T _j = 125°C, Vs2 = 4.3 V (Note 6)	-	-	0.8	
		T _j = 150°C	-	-	0.7	

- **twake_filt** テスト条件が追加されました

rev.0:

t _{wake_filt}	Dominant time for wake-up via bus		0.15	-	1.8	μs
------------------------	-----------------------------------	--	------	---	-----	----

rev.1:

t _{wake_filt}	Dominant time for wake-up via bus	CAN_EN = low	0.15	-	1.8	μs
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- **編集上の変更**

この変更は、製品の形状、適合性、または機能には影響しません。

影響を受ける部品の一覧:

注: 標準の部品番号(既製品)のみが部品一覧に記載されます。本 PCN に影響を受けるカスタム 部品は、PCN メールのお客様の特定の PCN の付属文書、または PCN カスタマイズポータルに記載されています。

NCV7450DB0R2G



Appendix A: Changed Products

Product	Customer Part Number	Qualification Vehicle	New Part Number	Replacement Supplier
NCV7450DB0R2G		NA		